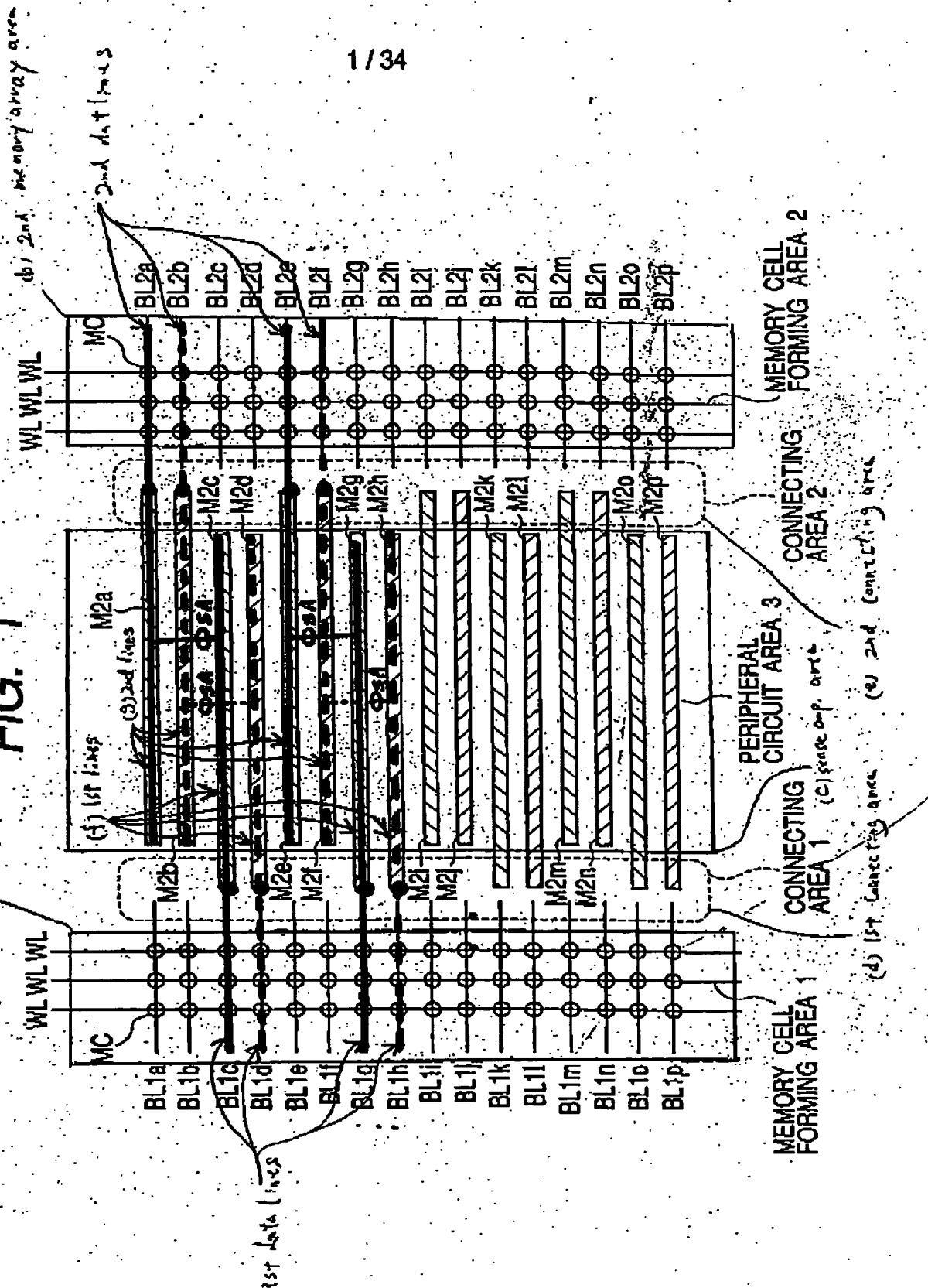


1/34

SKETCH I.

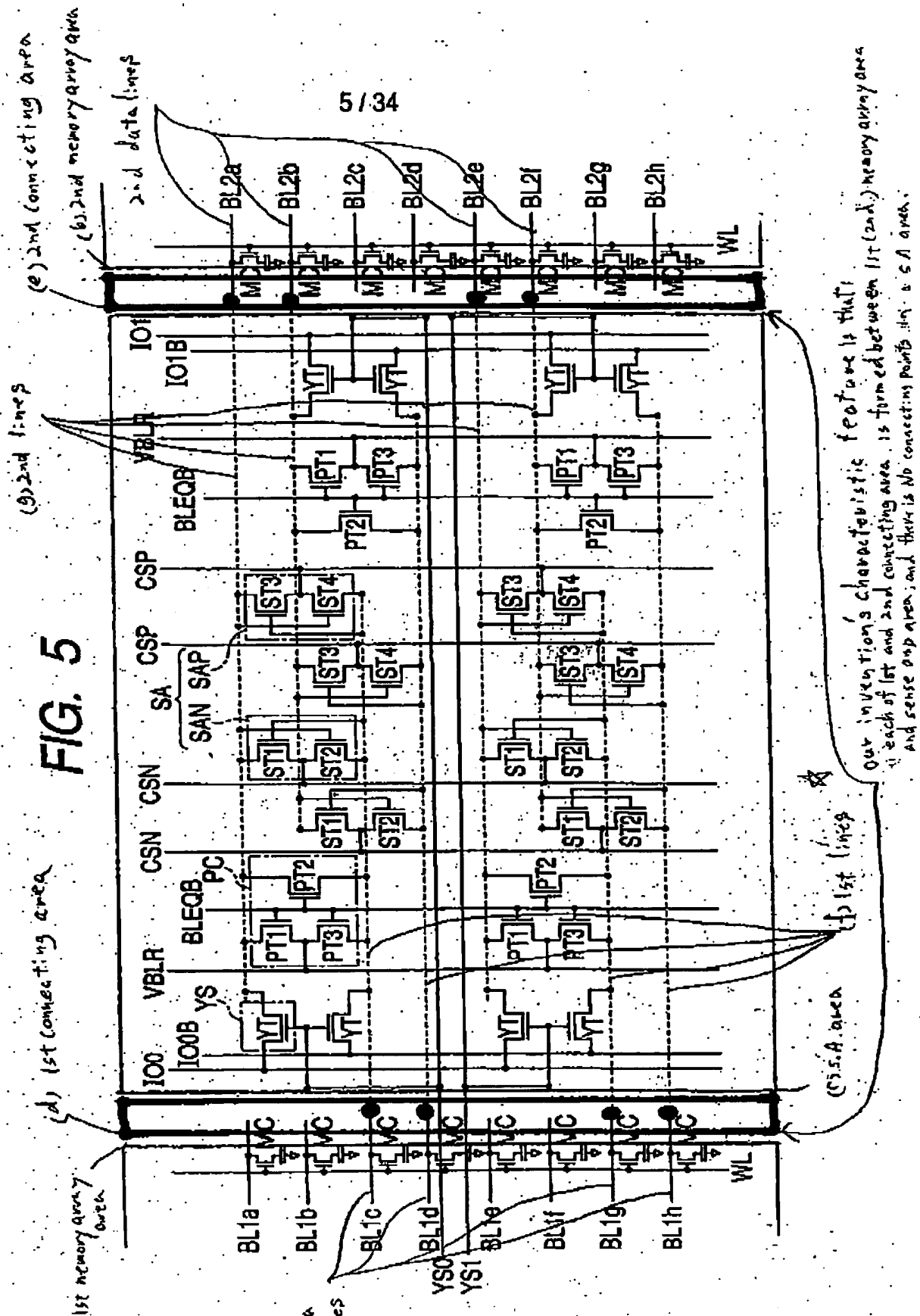
(a) 1st memory array area

FIG. 1



SKETCH 2:

FIG. 5

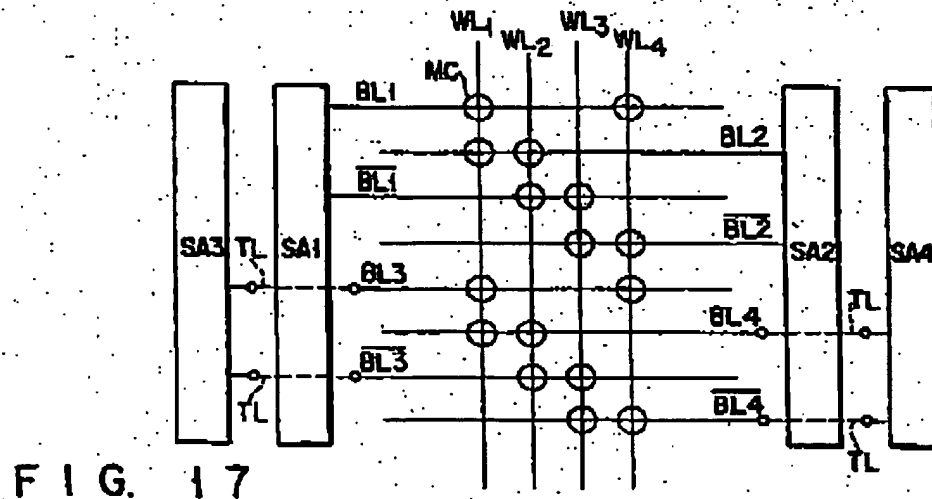
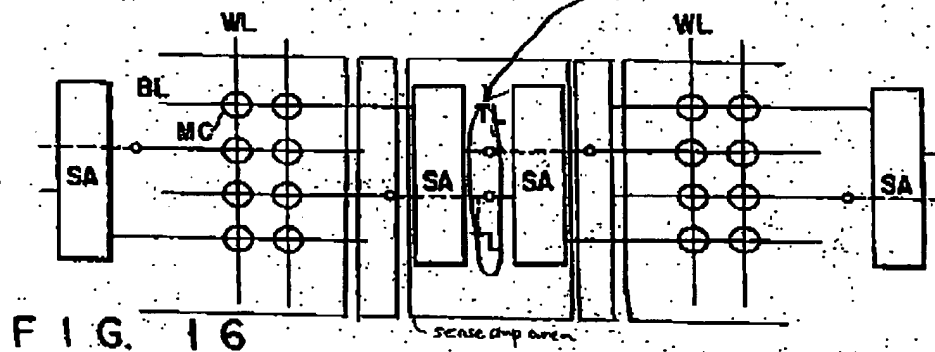
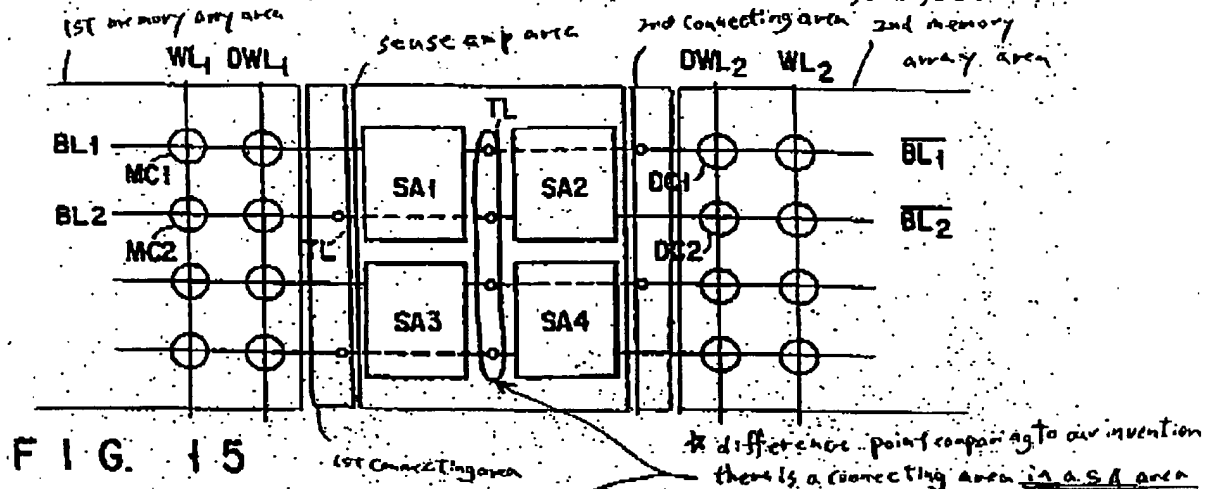


U.S. Patent

May 13, 1997

Sheet 12 of 20

5,629,887



SKETCH 3